FIG. 1

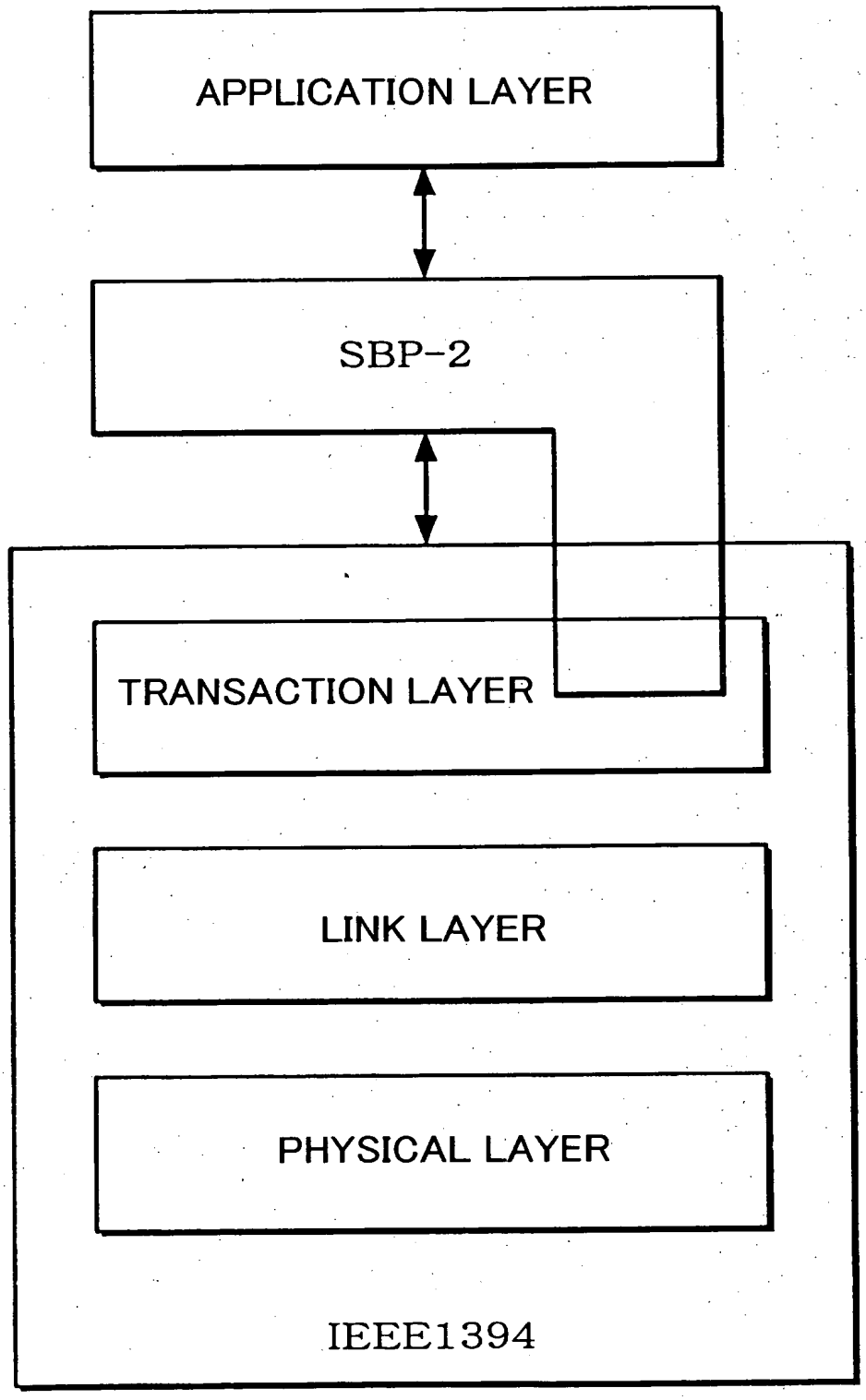
APPLICATION LAYER
SBP-2
TRANSACTION LAYER
LINK LAYER
PHYSICAL LAYER
IEEE1394

FIG. 2

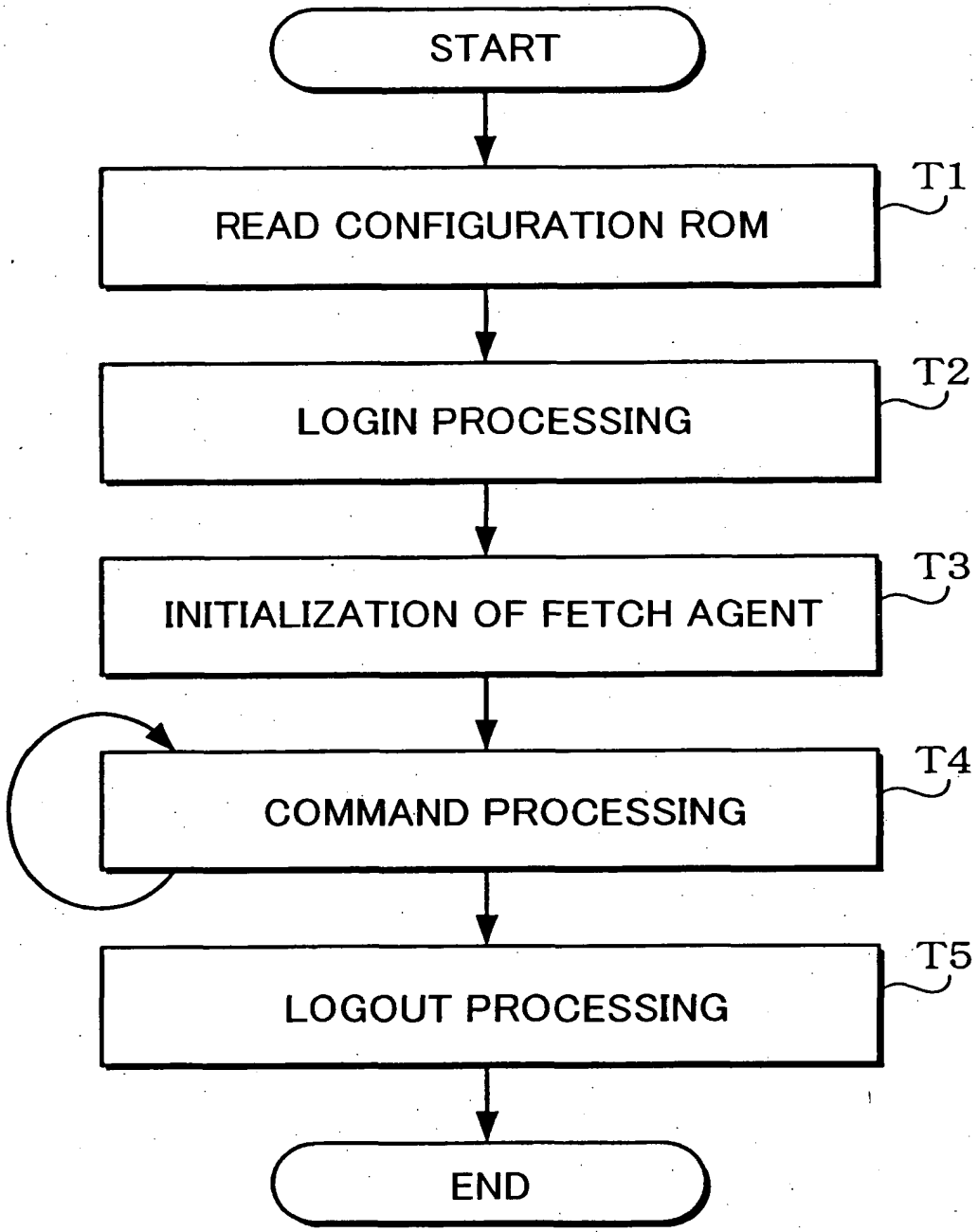
START
READ CONFIGURATION ROM
T1
LOGIN PROCESSING
T2
INITIALIZATION OF FETCH AGENT
T3
COMMAND PROCESSING
T4
LOGOUT PROCESSING
T5
END

FIG. 3

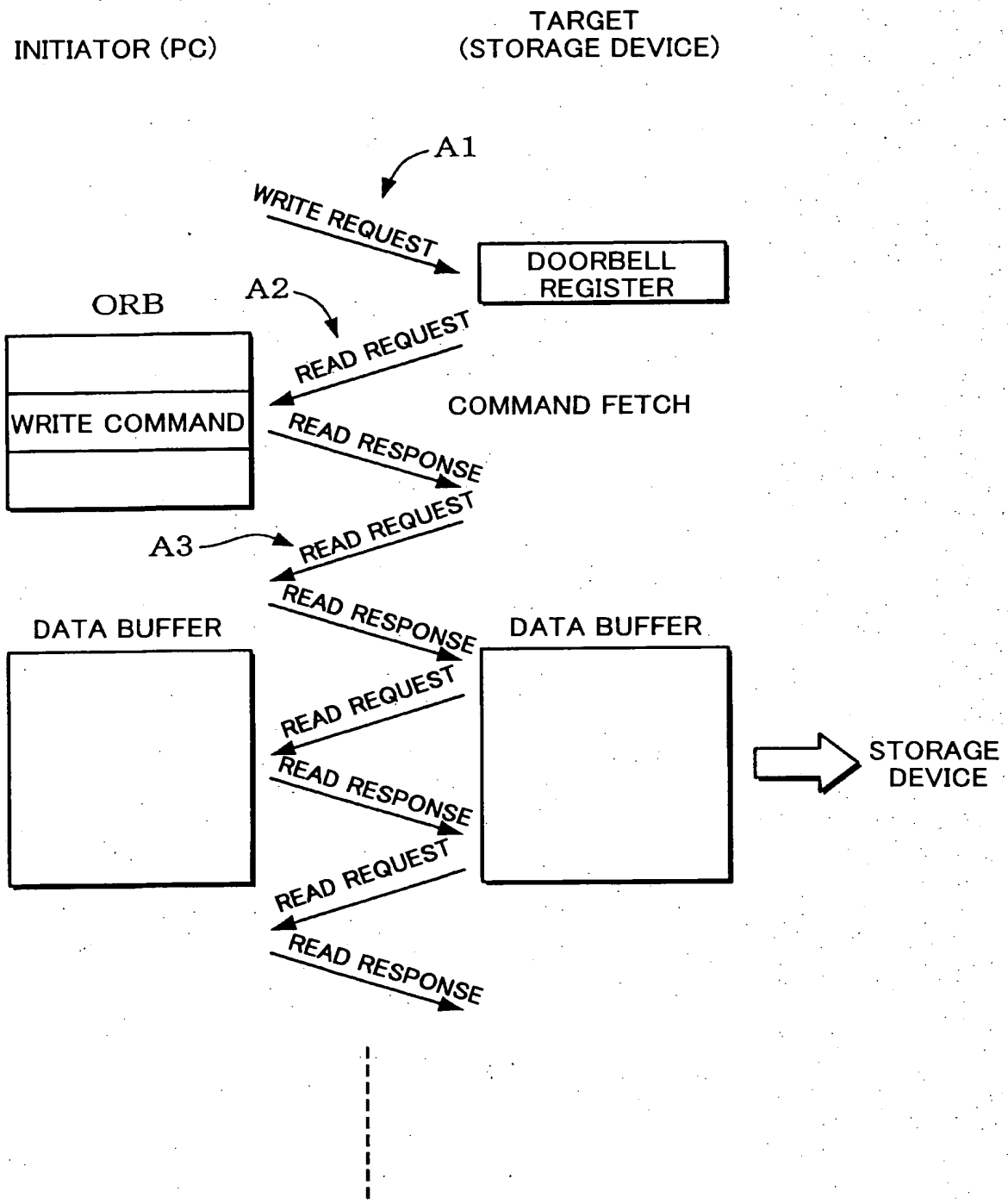
INITIATOR (PC)
TARGET
(STORAGE DEVICE)
A1
WRITE REQUEST
DOORBELL
REGISTER
ORB
A2
READ REQUEST
WRITE COMMAND
COMMAND FETCH
READ RESPONSE
A3
READ REQUEST
READ RESPONSE
DATA BUFFER
DATA BUFFER
READ REQUEST
READ RESPONSE
STORAGE
DEVICE
READ REQUEST
READ RESPONSE

FIG. 4

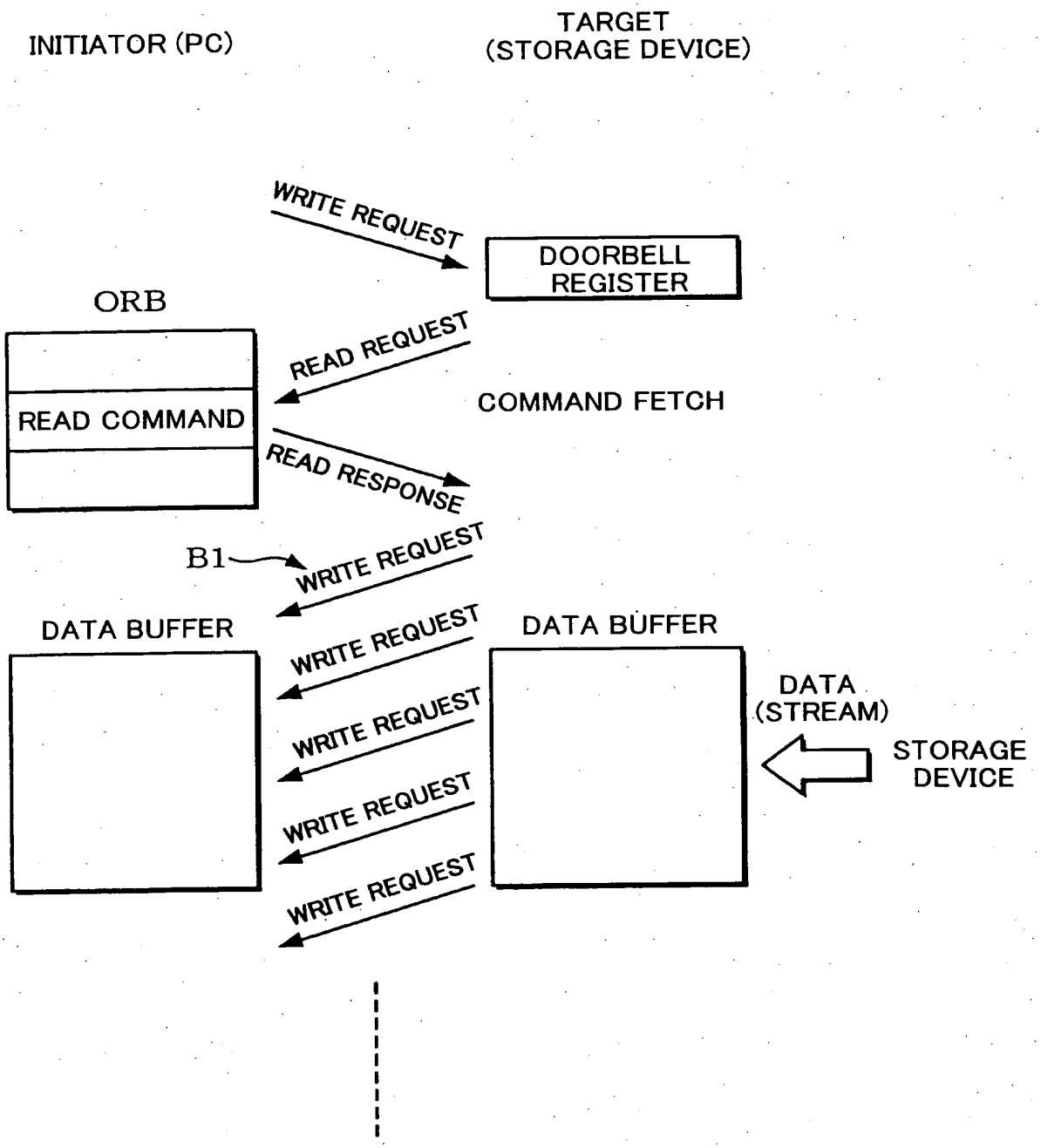
INITIATOR (PC)
TARGET
(STORAGE DEVICE)
WRITE REQUEST
DOORBELL
REGISTER
ORB
READ REQUEST
READ COMMAND
COMMAND FETCH
READ RESPONSE
B1
WRITE REQUEST
DATA BUFFER
WRITE REQUEST
DATA BUFFER
WRITE REQUEST
DATA
(STREAM)
WRITE REQUEST
STORAGE
DEVICE
WRITE REQUEST

FIG. 5A

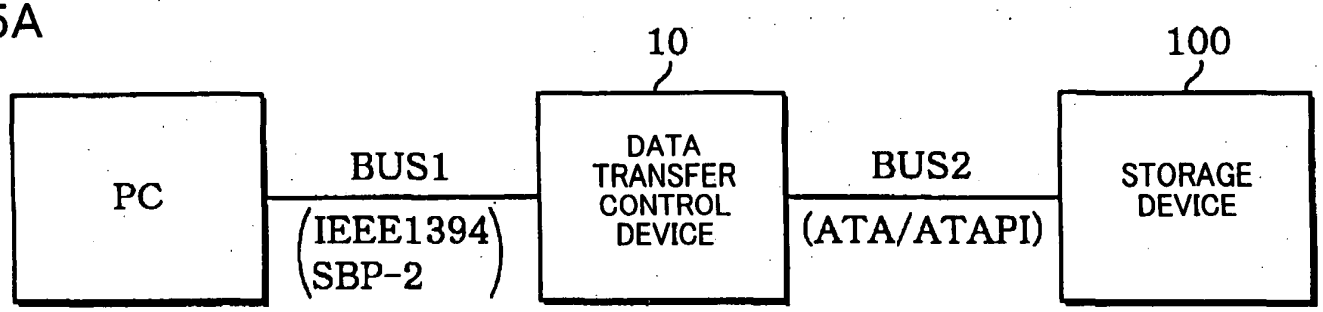

FIG. 5B DURING FABRICATION (DOWNLOAD MODE)

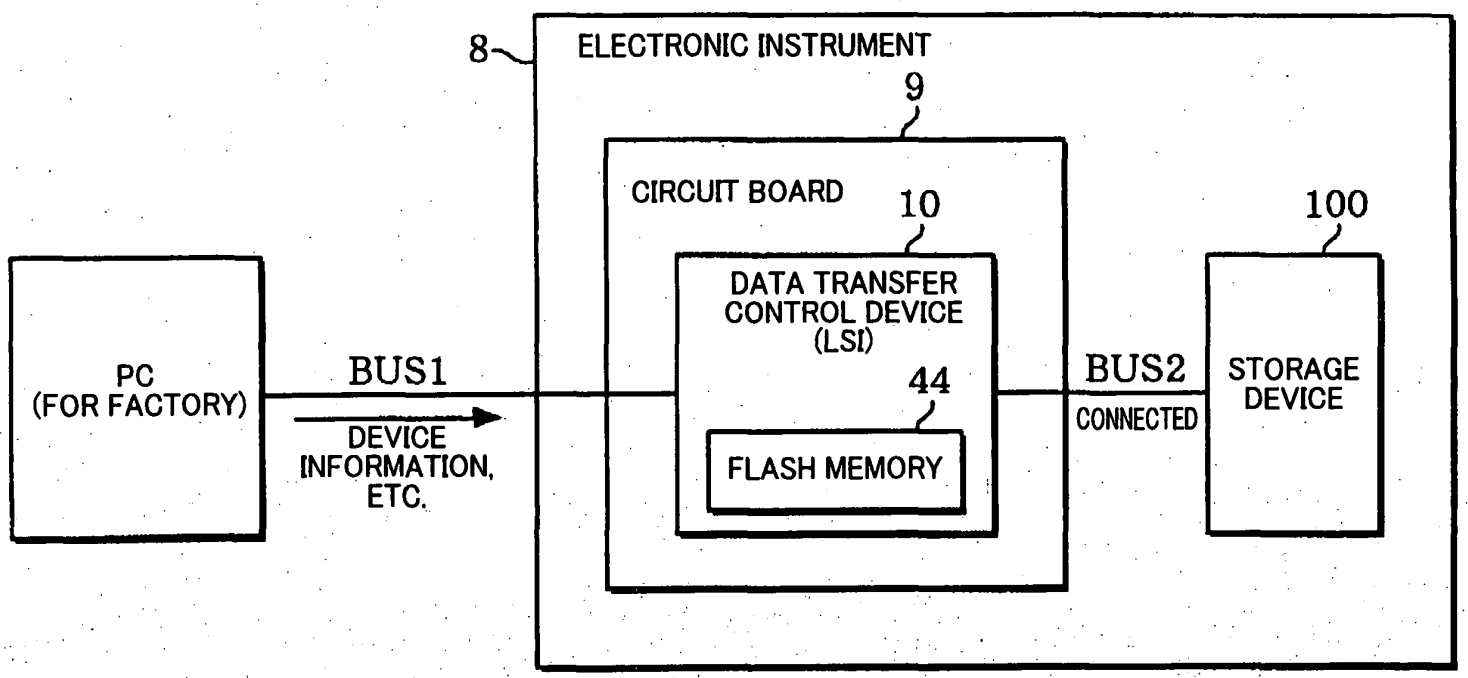

FIG. 6

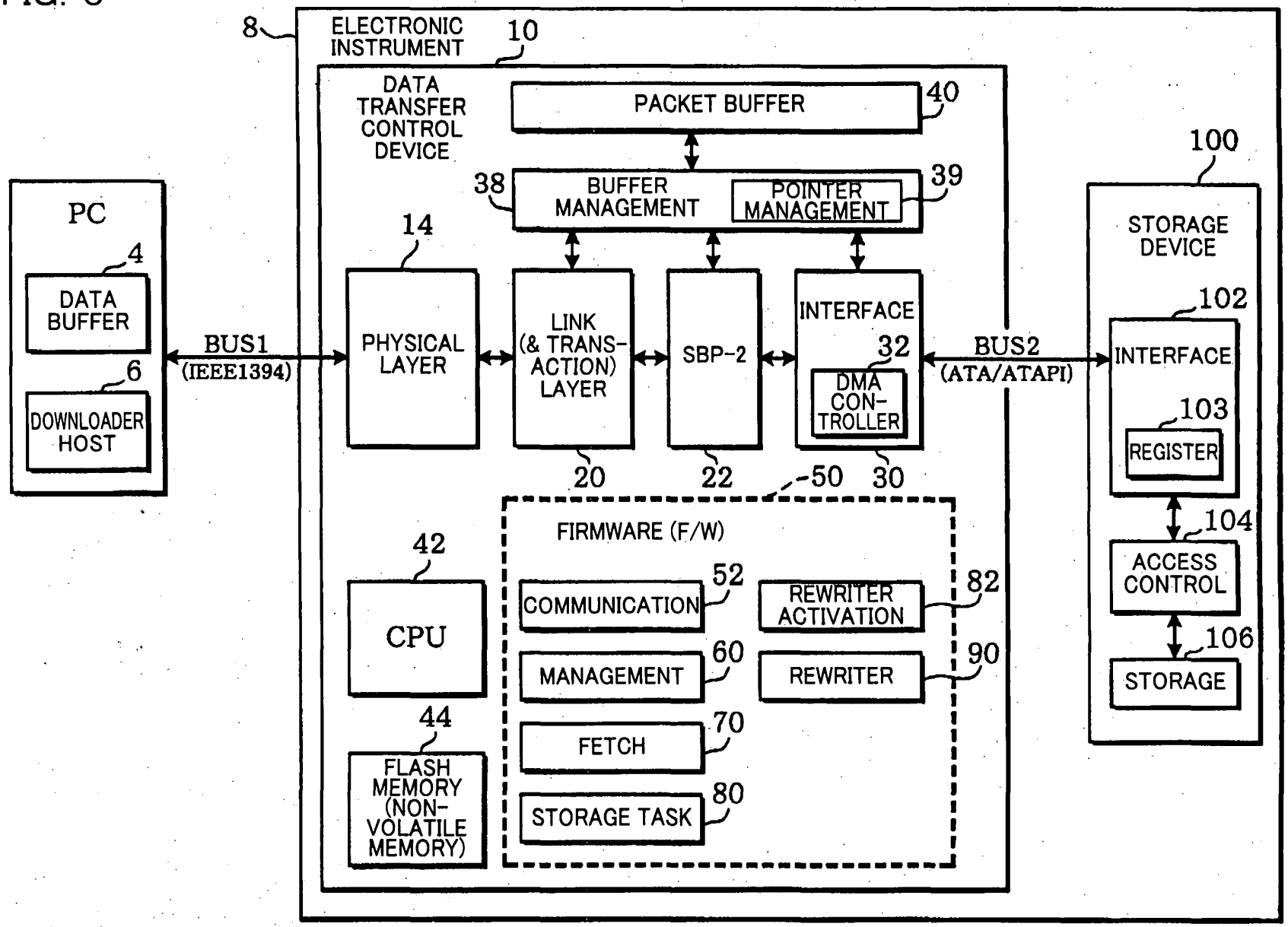
8
ELECTRONIC INSTRUMENT
10
DATA TRANSFER CONTROL DEVICE
PACKET BUFFER
40
38
BUFFER MANAGEMENT
POINTER MANAGEMENT
39
14
PC
4
DATA BUFFER
6
DOWNLOADER HOST
BUS1
(IEEE1394)
PHYSICAL LAYER
LINK (& TRANS-ACTION) LAYER
SBP-2
INTERFACE
32
DMA CON-TROLLER
20
22
50
30
FIRMWARE (F/W)
42
CPU
44
FLASH MEMORY (NON-VOLATILE MEMORY)
COMMUNICATION
52
MANAGEMENT
60
FETCH
70
STORAGE TASK
80
REWRITER ACTIVATION
82
REWRITER
90
BUS2
(ATA/ATAPI)
100
STORAGE DEVICE
102
INTERFACE
103
REGISTER
104
ACCESS CONTROL
106
STORAGE

FIG. 7

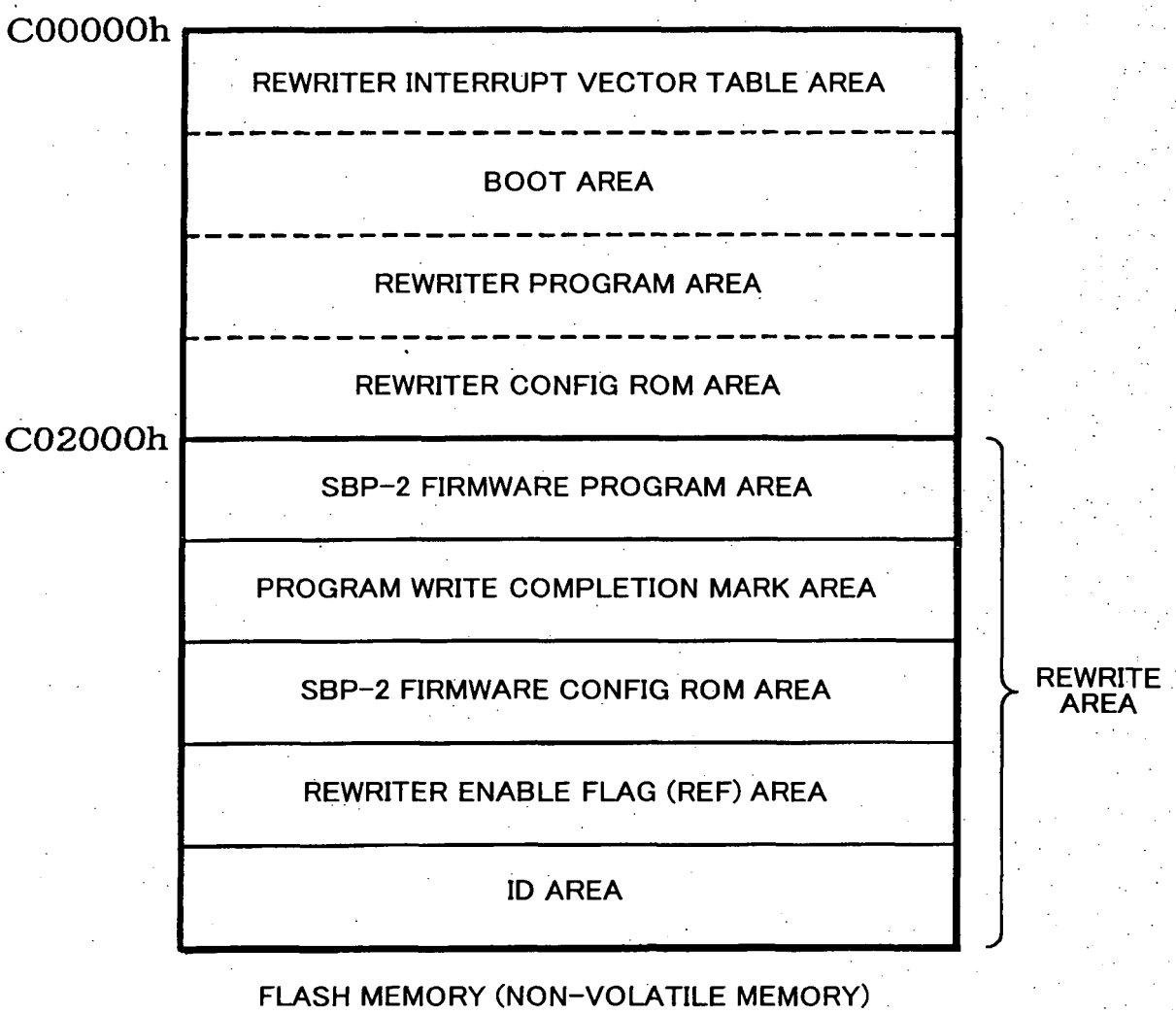
C00000h
REWRITER INTERRUPT VECTOR TABLE AREA
BOOT AREA
REWRITER PROGRAM AREA
REWRITER CONFIG ROM AREA
C02000h
SBP-2 FIRMWARE PROGRAM AREA
PROGRAM WRITE COMPLETION MARK AREA
SBP-2 FIRMWARE CONFIG ROM AREA
REWRITE AREA
REWRITER ENABLE FLAG (REF) AREA
ID AREA
FLASH MEMORY (NON-VOLATILE MEMORY)

FIG. 8

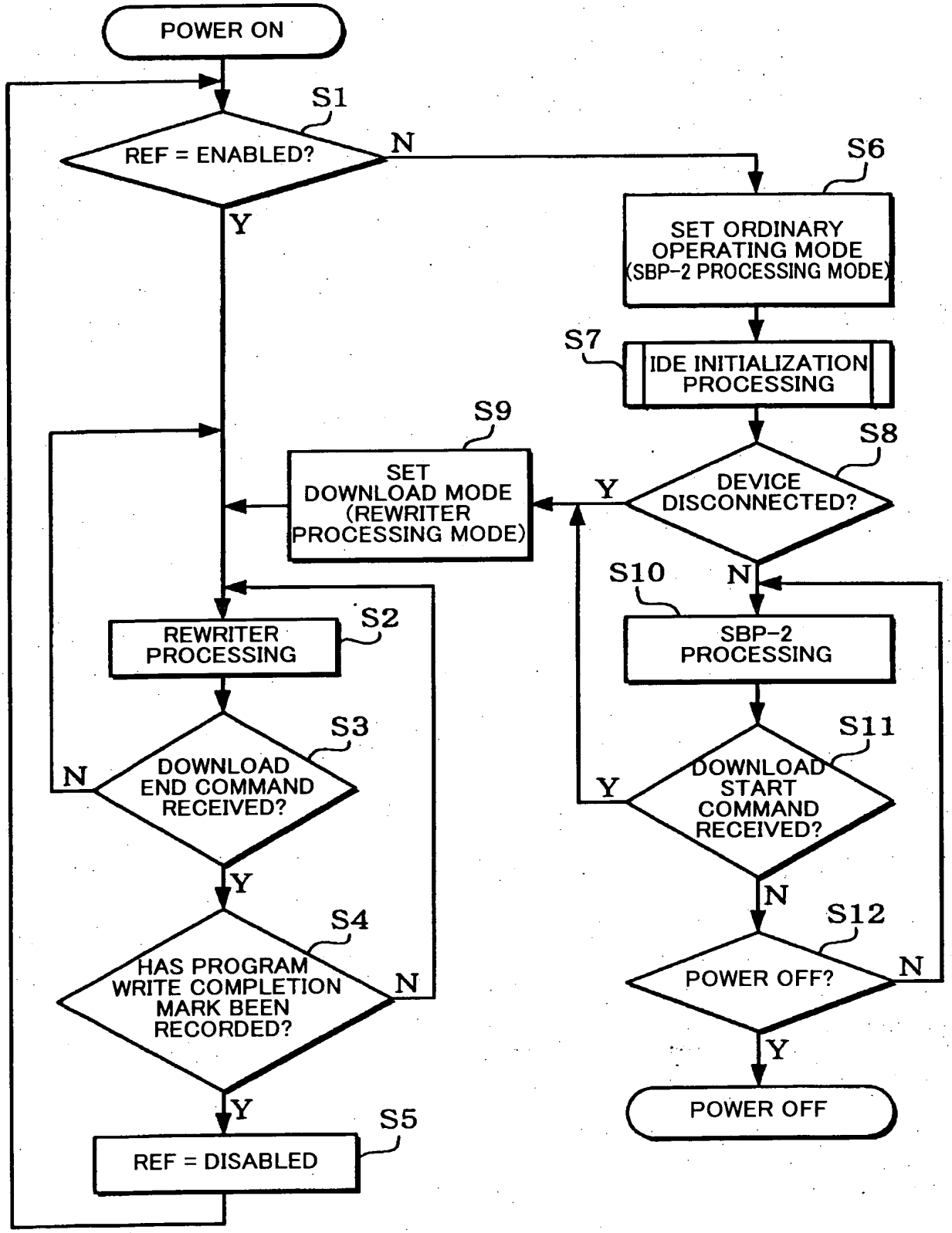
POWER ON
S1
REF = ENABLED?
N
Y
S6
SET ORDINARY OPERATING MODE (SBP-2 PROCESSING MODE)
S7
IDE INITIALIZATION PROCESSING
S8
DEVICE DISCONNECTED?
Y
S9
SET DOWNLOAD MODE (REWRITER PROCESSING MODE)
N
S10
SBP-2 PROCESSING
S11
DOWNLOAD START COMMAND RECEIVED?
Y
N
S12
POWER OFF?
N
Y
POWER OFF
S2
REWRITER PROCESSING
S3
DOWNLOAD END COMMAND RECEIVED?
N
Y
S4
HAS PROGRAM WRITE COMPLETION MARK BEEN RECORDED?
N
Y
S5
REF = DISABLED

FIG. 9

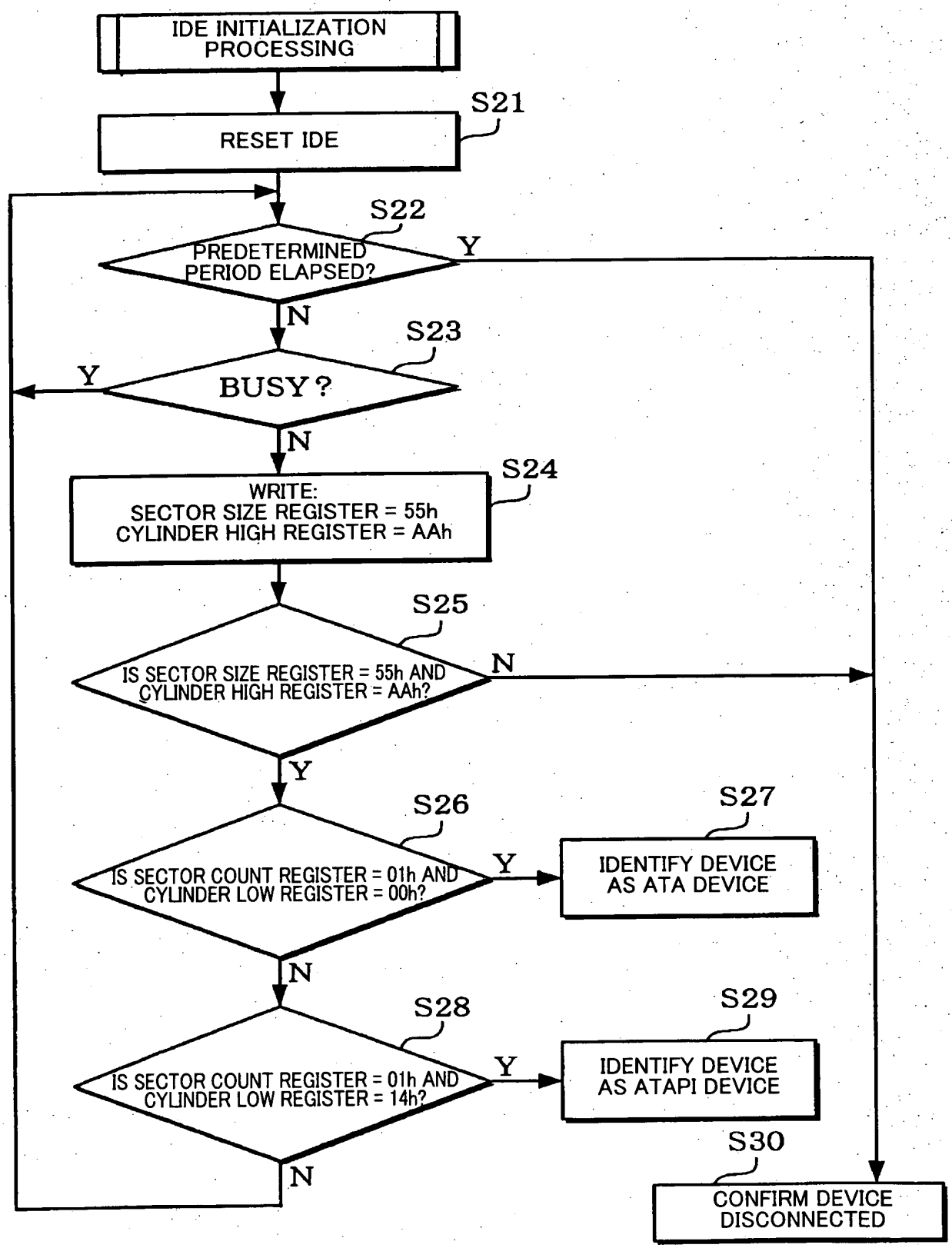
IDE INITIALIZATION PROCESSING
S21
RESET IDE
S22
PREDETERMINED PERIOD ELAPSED?
Y
N
S23
BUSY?
Y
N
S24
WRITE:
SECTOR SIZE REGISTER = 55h
CYLINDER HIGH REGISTER = AAh
S25
IS SECTOR SIZE REGISTER = 55h AND CYLINDER HIGH REGISTER = AAh?
N
Y
S26
IS SECTOR COUNT REGISTER = 01h AND CYLINDER LOW REGISTER = 00h?
Y
S27
IDENTIFY DEVICE AS ATA DEVICE
N
S28
IS SECTOR COUNT REGISTER = 01h AND CYLINDER LOW REGISTER = 14h?
Y
S29
IDENTIFY DEVICE AS ATAPI DEVICE
N
S30
CONFIRM DEVICE DISCONNECTED

FIG. 10A

STATUS REGISTER

7	6	5	4	3	2	1	0
BSY	DRDY	#	#	DRQ	obs	obs	ERR

FIG. 10B ATA

REGISTER	
SECTOR COUNTER	01h
SECTOR NUMBER	01h
CYLINDER LOW	00h
CYLINDER HIGH	00h
DEVICE/HEAD	00h

FIG. 10C ATAPI

REGISTER	
SECTOR COUNTER	01h
SECTOR NUMBER	01h
CYLINDER LOW	14h
CYLINDER HIGH	EBh
DEVICE/HEAD	00h OR 10h

FIG. 11A DURING FABRICATION (DOWNLOAD MODE)

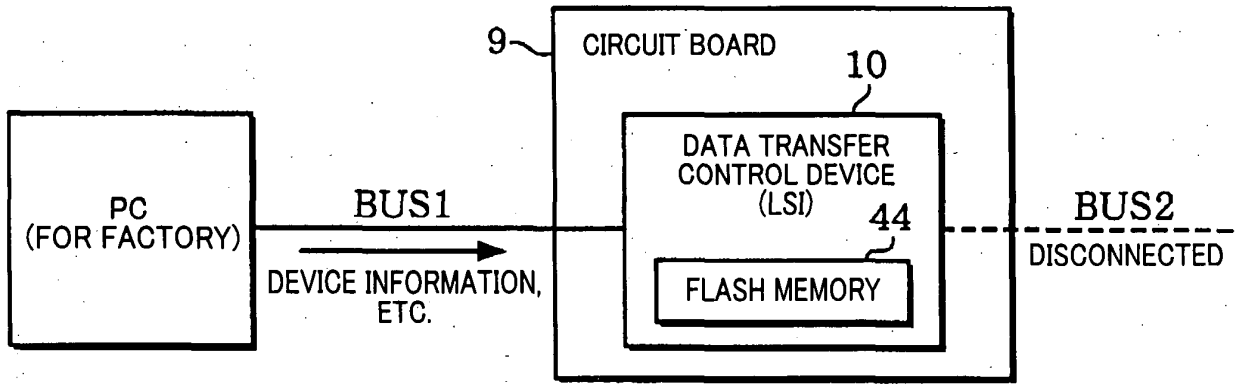

FIG. 11B DURING FABRICATION (INCORPORATION OF CIRCUIT BOARD)

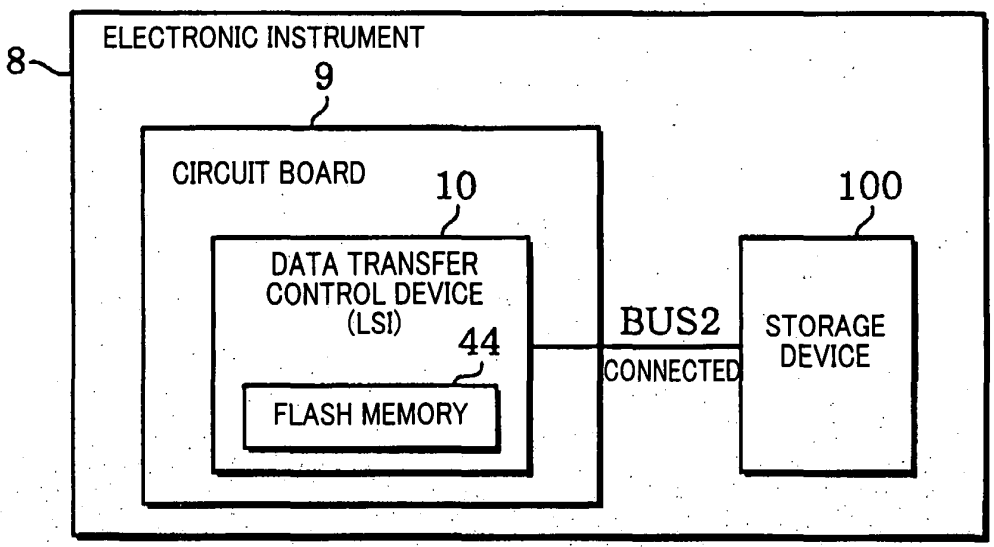

FIG. 12A

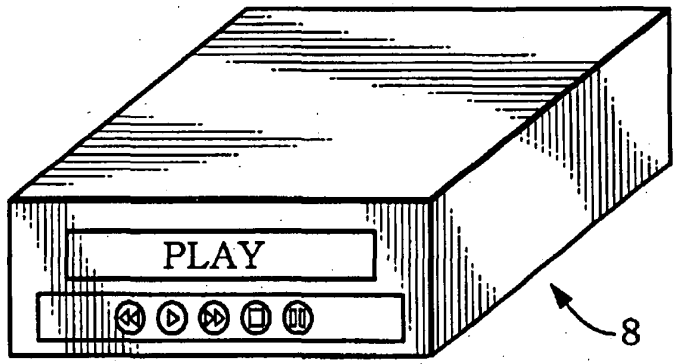

FIG. 12B DURING USE (ORDINARY OPERATING MODE)

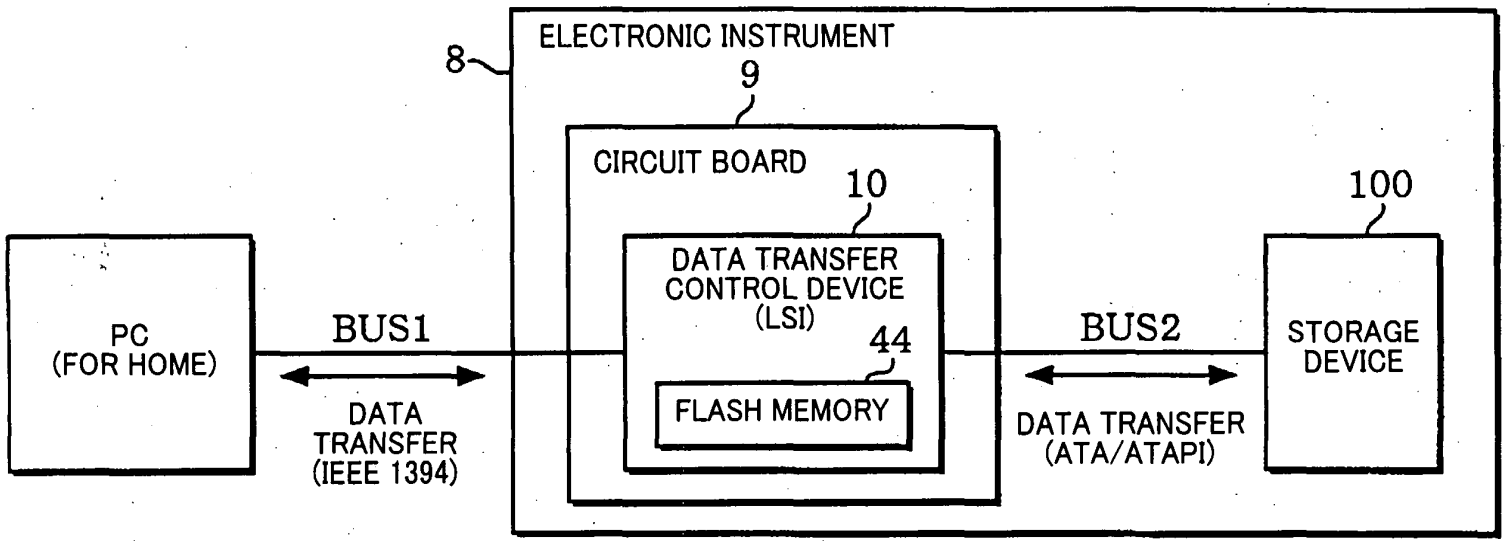

FIG. 13

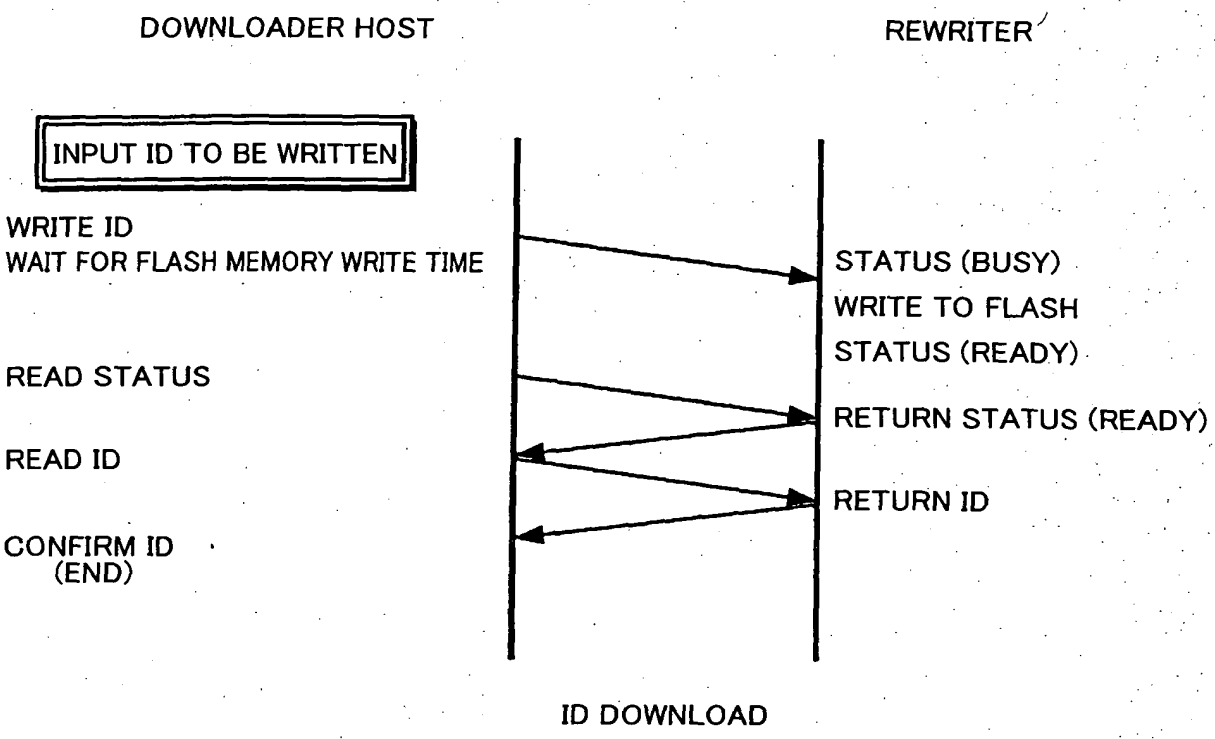
DOWNLOADER HOST
REWRITER
INPUT ID TO BE WRITTEN
WRITE ID
WAIT FOR FLASH MEMORY WRITE TIME
STATUS (BUSY)
WRITE TO FLASH
STATUS (READY)
READ STATUS
RETURN STATUS (READY)
READ ID
RETURN ID
CONFIRM ID
(END)
ID DOWNLOAD

FIG. 14

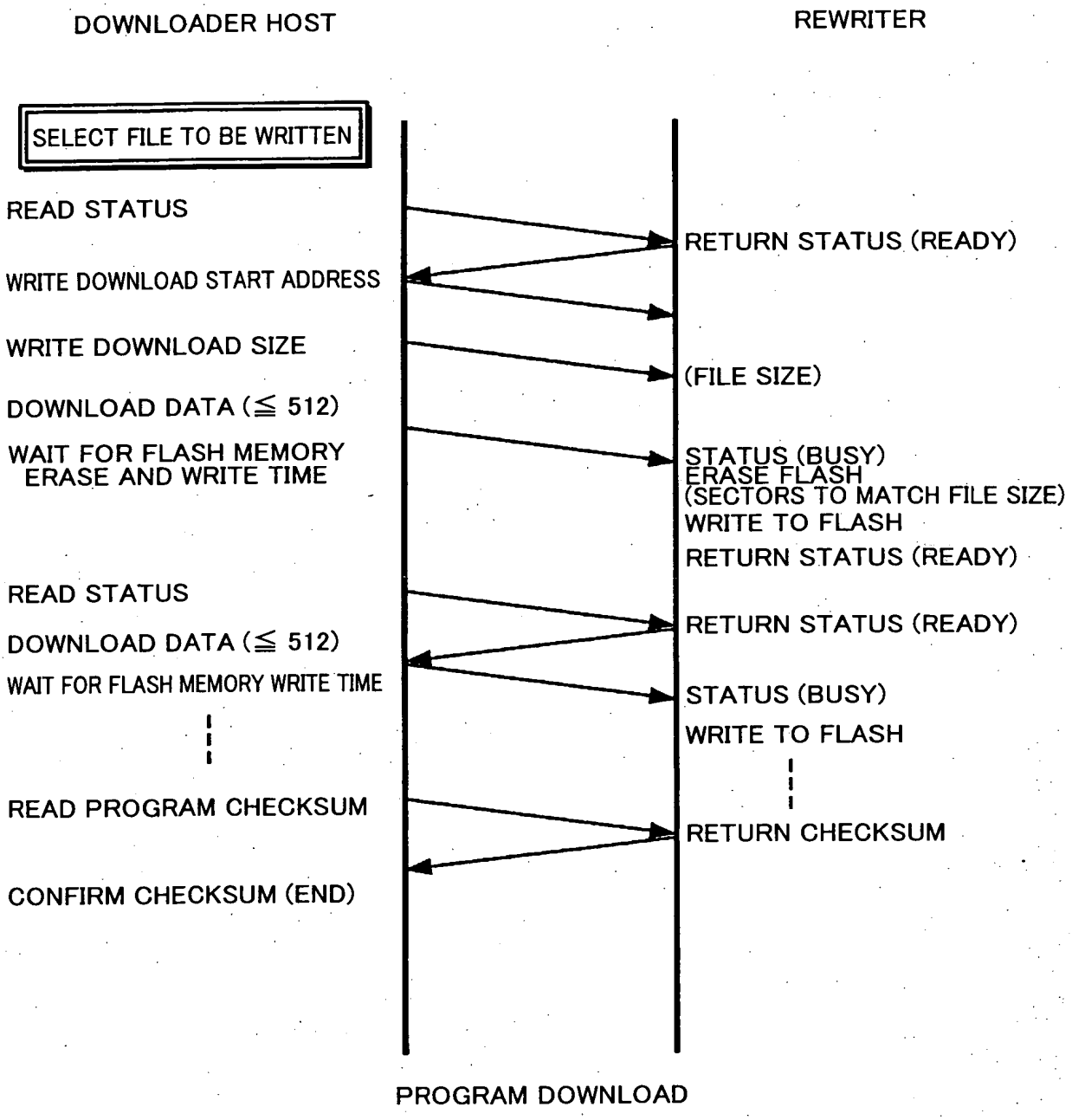
DOWNLOADER HOST
REWRITER
SELECT FILE TO BE WRITTEN
READ STATUS
RETURN STATUS (READY)
WRITE DOWNLOAD START ADDRESS
WRITE DOWNLOAD SIZE
(FILE SIZE)
DOWNLOAD DATA (≦ 512)
WAIT FOR FLASH MEMORY ERASE AND WRITE TIME
STATUS (BUSY)
ERASE FLASH
(SECTORS TO MATCH FILE SIZE)
WRITE TO FLASH
RETURN STATUS (READY)
READ STATUS
RETURN STATUS (READY)
DOWNLOAD DATA (≦ 512)
WAIT FOR FLASH MEMORY WRITE TIME
STATUS (BUSY)
WRITE TO FLASH
READ PROGRAM CHECKSUM
RETURN CHECKSUM
CONFIRM CHECKSUM (END)
PROGRAM DOWNLOAD

FIG. 15A

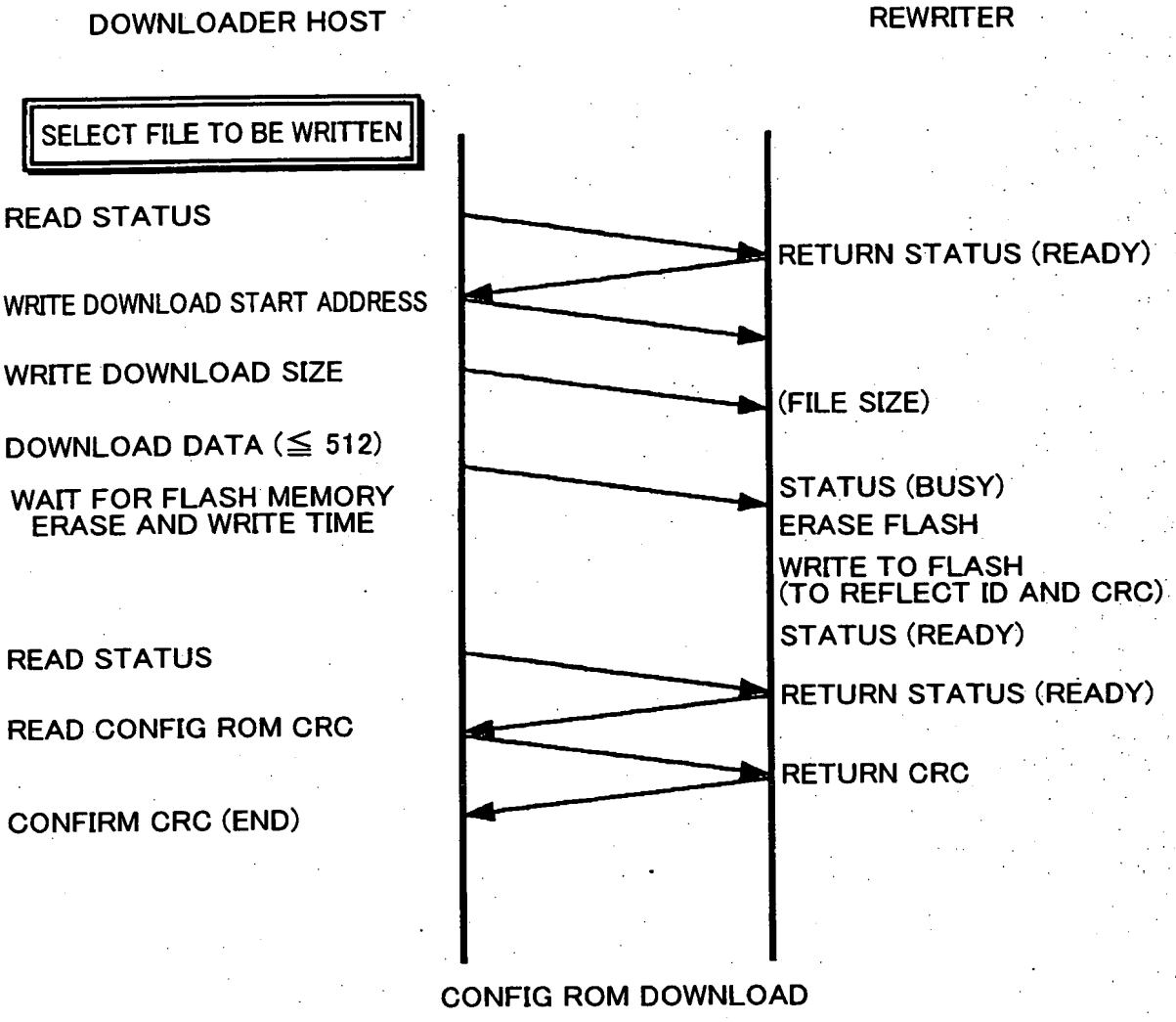

FIG. 15B

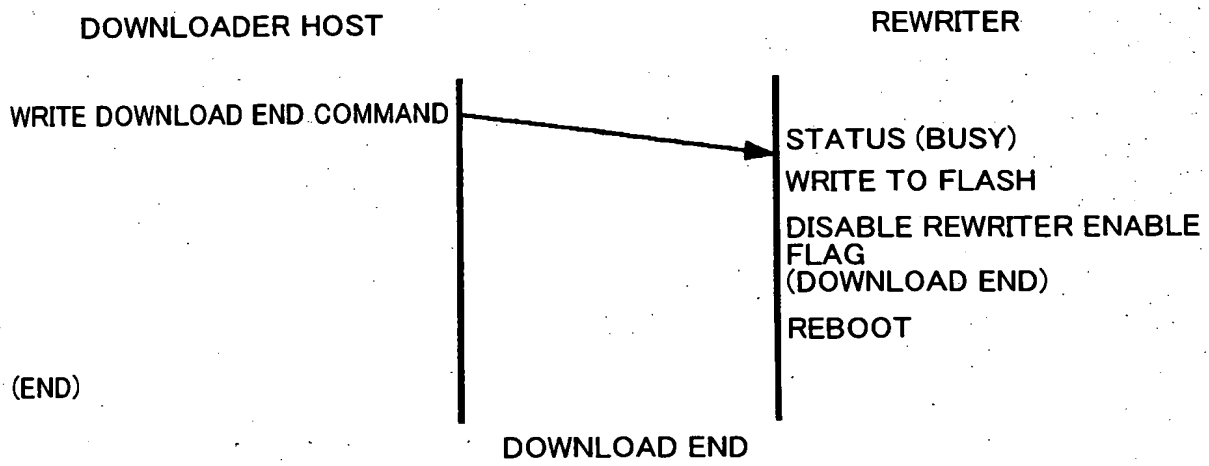

FIG. 16

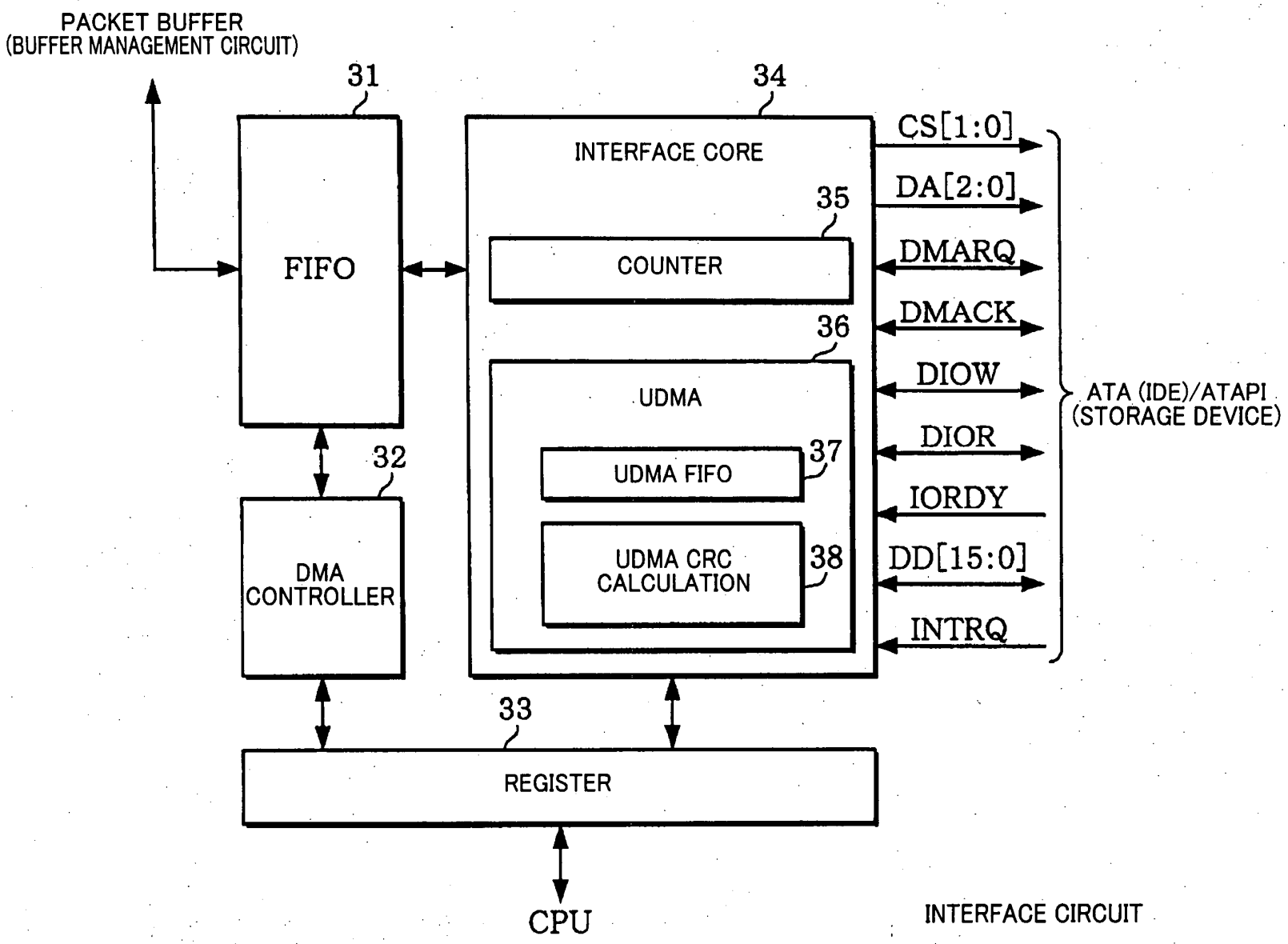
PACKET BUFFER
(BUFFER MANAGEMENT CIRCUIT)
31
34
FIFO
INTERFACE CORE
35
COUNTER
36
UDMA
37
UDMA FIFO
38
UDMA CRC
CALCULATION
32
DMA
CONTROLLER
33
REGISTER
CPU
CS[1:0]
DA[2:0]
DMARQ
DMACK
DIOW
DIOR
IORDY
DD[15:0]
INTRQ
ATA (IDE)/ATAPI
(STORAGE DEVICE)
INTERFACE CIRCUIT

FIG. 17A

PIO READ (STORAGE DEVICE → DATA TRANSFER CONTROL DEVICE → PC)

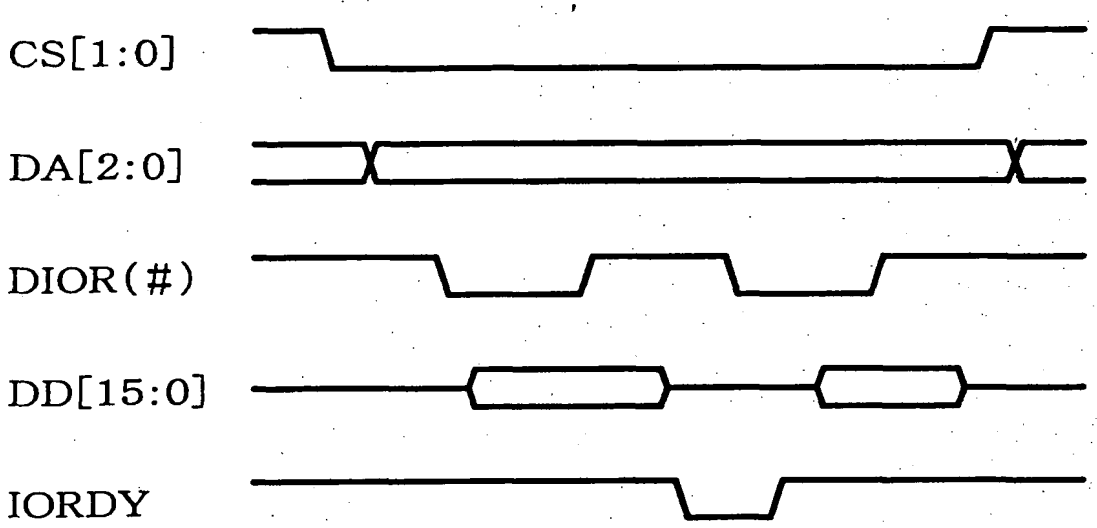

FIG. 17B

PIO WRITE (PC → DATA TRANSFER CONTROL DEVICE → STORAGE DEVICE)